REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 15, 19, and 38-72 are in this application. Claims 40-44, 58-59, 63-64, and 67-68 have been allowed. Claims 1-14, 16-18, and 20-37 have been cancelled.

The Examiner rejected claims 15, 19, 38-39, 45-57, 60-62, 65-66, and 69-72 under 35 U.S.C. §103(a) as being unpatentable over Gens et al. (U.S. Patent No. 5,515,225) considered alone, or in view of the Admitted Prior Art (APA). For the reasons set forth below, applicant respectfully does not understand the Examiner's rejection.

With respect to claims 15 and 57, in the previous Office Action (May 29, 2003), the Examiner argued that the lines that are connected to the right sides of the high power supply terminals labeled VDD1 and VDD2 shown in FIG. 2 of Gen's structure could be read to be the plurality of positive lines required by claims 15 and 57. In the previous amendment (October 27, 2003), applicant noted that the power supply terminals VDD1 and VDD2 were pads. As a result, the lines identified by the Examiner could not be read to be the positive lines required by claims 15 and 57, which expressly recite that none of the positive lines are directly connected to a pad.

In the present Office Action (February 13, 2004), the Examiner stated that "[A]pplicant's arguments with respect to claims 15, 19, 38-39, 45-57, 60-62, 65-66 and 69-72 have been considered but are moot in view of the new ground(s) of rejection." In addition, the Examiner does not appear to have addressed any of applicant's arguments with respect to claims 15 and 57.

In view of the Examiner's moot statement and the absence of a response to applicant's arguments, applicant assumes that the Examiner agrees that the lines connected to the power supply terminals VDD1 and VDD2 can not be read to be the plurality of positive lines required by claims 15 and 57, and the only pending arguments are the new ground(s) of rejection set forth in the present Office Action.

However, the only new ground of rejection set forth by the Examiner for claims 15 and 57 reads as follows:

> "The embodiment of figure 3 depicts a plurality of ESD positive lines being directly connected to VDD pads. Gen et al. teach that an artisan can modify the device by connecting a pair of parallel head to tail diodes between each high voltage supply (VDD) and the bus (R1) (column 4, lines 28-36). It would also have been obvious to a person of ordinary skill in the art at the time the invention was made to connect a pair of parallel head to tail diodes between each high voltage supply (VDD) and the bus (R1) in Gens et al.'s device in order to improve the isolation between the various power supply sources."

If the Examiner agrees that the lines connected to the power supply terminals VDD1 and VDD2 can not be read to be the plurality of positive lines required by claims 15 and 57, and that the Gens reference does not teach a plurality of structures which can be read to be the plurality of positive lines, then the Examiner must identify where in the Gens structure a plurality of positive lines could be added in a way that satisfies the claim limitations, and argue why one skilled in the art would be motivated to place the positive lines in this location to establish a prima facia case of obviousness.

However, applicant respectfully can not determine the location where the Examiner is suggesting that a plurality of positive lines would be added to the Gens structure, or why one skilled in the art would be motivated to make this modification to the Gens circuit.

FIGS. 2 and 3 of Gens show a single head-to-toe diode D1 connected between the power supply terminal VDD1 and the bus R1. The Examiner argued that it would obvious to use a pair of parallel head-to-toe diodes in lieu of a single diode D1, citing column 4, lines 28-36 of Gens. Applicant respectfully does not understand how using two diodes in parallel changes anything. The inputs of both parallel diodes are still connected to the high voltage pad VDD1, and the outputs of both parallel diodes are still connected to bus R1.

Thus, since the Examiner did not identify a location where a plurality of positive lines could be added to the Gens structure, or why one skilled in the art would be motivated to make this modification to the Gens circuit, the Examiner has not set forth a prima facia case

of obviousness. As a result, claims 15 and 57 are patentable over Gens, and Gens in view of the Admitted Prior Art (APA). In addition, since claims 19, 38, 39, 45-50, and 69 and claims 60, 61, and 70 depend either directly or indirectly from claim 15, claims 19, 38, 39, 45-50, and 69 and claims 60. 61, and 70, respectively, are patentable over Gens for the same reasons as claims 15 and 57.

With respect to claims 51 and 62, in the previous Office Action (May 29, 2003), the Examiner argued that it would be obvious to replace a lower diode (e.g., the diode D2 that is connected to pad VDD1 shown in FIG. 2 of Gens) with a switch or a transistor. This argument, however, is based on the assumption that the lines connected to the high voltage pads VDD1 and VDD2 can be read to be the positive lines of the claims. However, as noted above, the lines connected to the high voltage pads VDD1 and VDD2 can not be read to be the positive lines of the claims.

Thus, since the Examiner did not identify a location where a plurality of positive lines could be added to the Gens structure, or why one skilled in the art would be motivated to make this modification to the Gens circuit, the Examiner has not set forth a prima facia case of obviousness. As a result, claims 51 and 62 are patentable over Gens, and Gens in view of the Admitted Prior Art (APA). In addition, since claims 52-56 and 71, and claims 65-66 and 72 depend either directly or indirectly from claims 51 and 62, respectively, claims 52-56 and 71 and claims 65-66 and 72 are patentable over Gens for the same reasons as claims 51 and 62.

Further, claims 51 and 62 also require that a switch pass a current from a positive line to the negative ring. The Examiner argued that it would be obvious to use a transistor, which can function as a switch, in lieu of a diode D2. In addition, the Examiner argued that one would be motivated to make this change in order to improve the switching capabilities of the device during an ESD event. However, the Examiner has not indicated how the use of a transistor would improve the switching capabilities. In addition, the change suggested by the Examiner would no longer allow a diode D2, or the entire circuit, or operate as intended.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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